	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	20076	phase near4 error$5	USPAT	2004/02/09 15:27	
2	BRS	L2	2135	1 same (calcul$5)	USPAT	2004/02/09 15:13	
3	BRS	L3	77	2 same (absolute adj5 value)	USPAT	2004/02/09 15:14	
4	BRS	L4	8	3 and ((detect$5 determ$5) same edge)	USPAT	2004/02/09 15:18	
5	BRS	L5	5	4 and (sampl$5 adj8 values)	USPAT	2004/02/09 15:18	
6	BRS	L7	0	4 and ((sampl$5 adj8 values) same continu$5)	USPAT	2004/02/09 15:19	
7	BRS	L8	1	4 and (calcula$5 same continu$5)	USPAT	2004/02/09 15:19	
8	BRS	L6	5	4 and (sampl$5 adj8 values)	USPAT	2004/02/09 15:23	
9	BRS	L10	2	4 and (sampl$5 same (second adj8 value$1))	USPAT	2004/02/09 15:24	
10	BRS	L9	1	4 and (sampl$5 same (first adj8 values))	USPAT	2004/02/09 15:26	
11	BRS	L11	16540	phase near4 error$5	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:27	
12	BRS	L12	1814	11 same (calcula$5)	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:27	
13	BRS	L13	54	12 same (absolute adj5 value)	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:27	

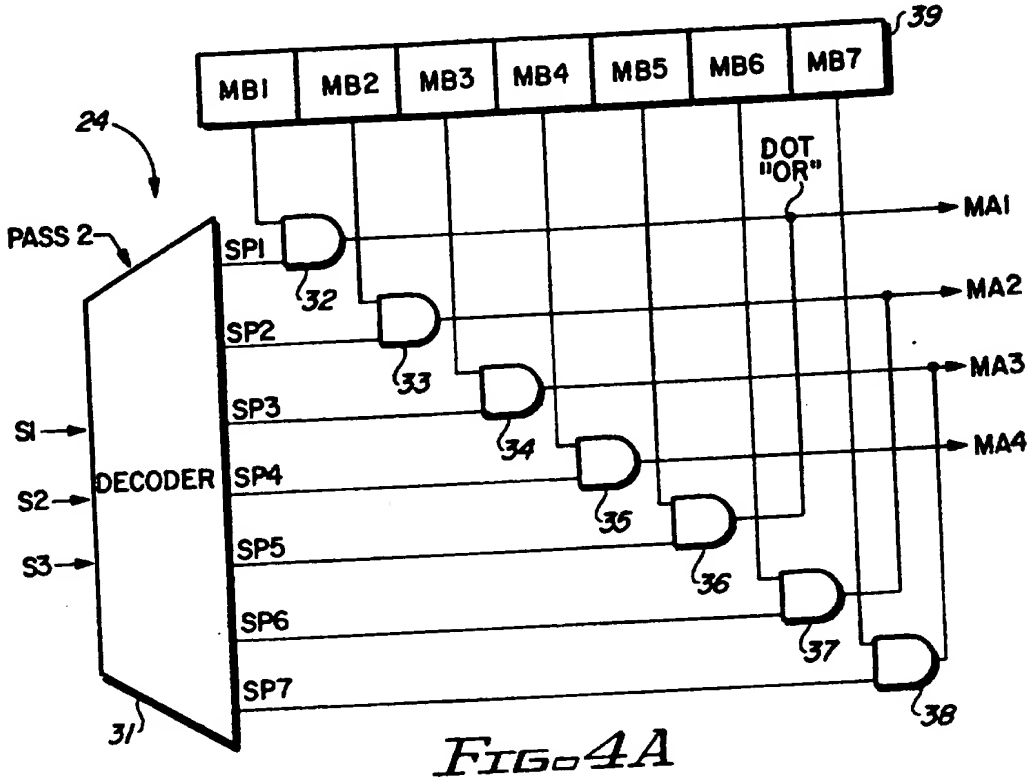

39
MB1
MB2
MB3
MB4
MB5
MB6
MB7
24
DOT "OR"
PASS 2
SP1
MA1
32
SP2
MA2
33
SP3
MA3
34
S1
SP4
MA4
DECODER
35
S2
36
SP5
S3
37
SP6
38
SP7
31

FIG. 4A

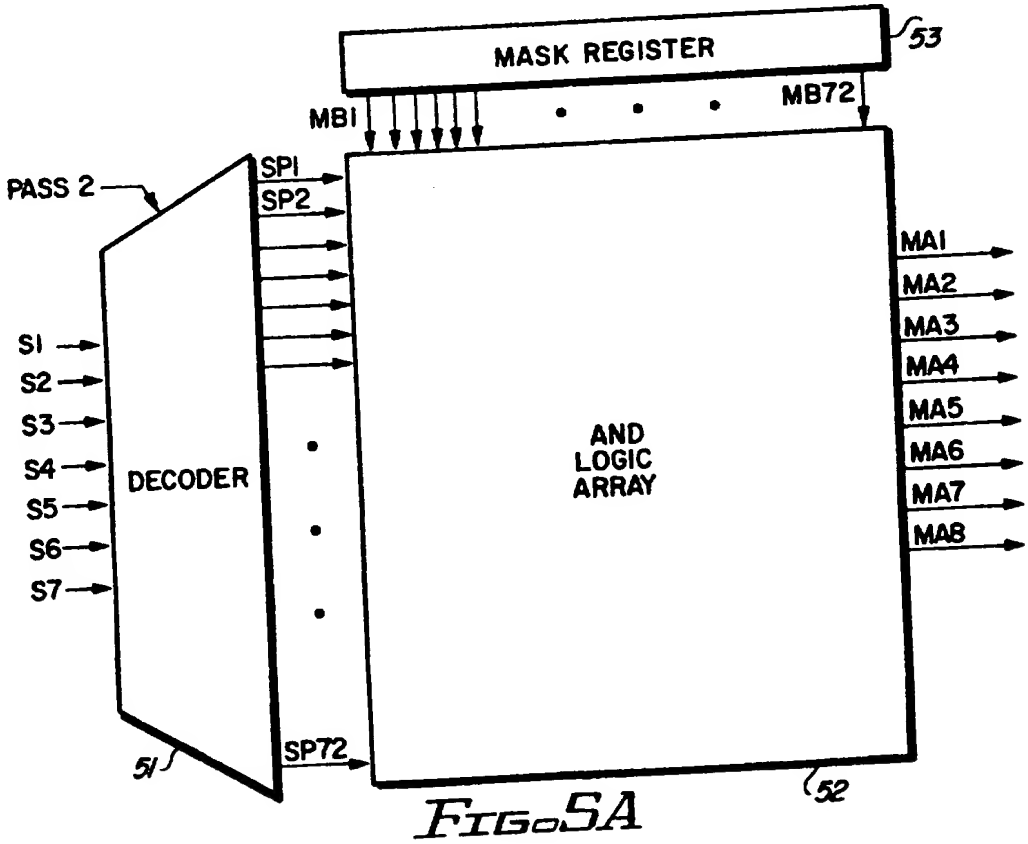

MASK REGISTER
53
MB1
MB72
PASS 2
SP1
SP2
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
S1
S2
S3
S4
S5
S6
S7
DECODER
AND LOGIC ARRAY
SP72
51
52

FIG. 5A

	Error Definition	Errors
1		0
2		0
3		0
4		0
5		0
6		0
7		0
8		0
9		0
10		0
11		0
12		0
13		0

FAULT MAPPING APPARATUS FOR MEMORY

FIELD OF THE INVENTION

This invention relates generally to the field of memory fault mapping, and more particularly to an apparatus and method of fault mapping memory while on-line.

BACKGROUND OF THE INVENTION

Computer systems traditionally use several different types of storage for retaining data. The ideal storage provides high speed writing and reading of data, has a low cost per unit of data stored, and stores the data reliably. Solid state electronic memory, hereinafter referred to as memory, has the characteristic of high speed access but the quantity of memory that can be provided is limited by its higher cost per unit of data. Memory is also volatile in that it loses the stored data when power is removed. Magnetic and optical disks can provide much greater storage capacity at a lower cost. Unlike memory, the magnetic and optical disks are nonvolatile in that data is retained in the absence of power. However, access to the data stored on magnetic and optical disks is much slower compared to memory. A higher storage capacity at yet a lower cost but with still slower access speed is provided by magnetic tape storage.

Increasing the speed at which a computer operates is a major driving force of every new generation of computers and the time to access or store data is a major factor in determining that speed. Hence there is a constant demand for increasing the amount of memory provided in today's computers. Using larger amounts of memory also increases the number of errors that are generated since an increased number of components are required and the increased probability of component failure necessarily follows. Requirements for reliability necessitate that a mechanism be provided for checking the contents of memory for accuracy and replacing faulty memory when found.

One technique of detecting and correcting errors in a memory is described in "Error Correction Technique Which Increases Memory Bandwidth and Reduces Access Penalties", IBM Technical Disclosure Bulletin, Vol. 31, No. 3, August 1988, pp. 146–149. This technique uses redundant memory banks where identical data is stored in each memory bank. Redundant memory has the advantage of correcting errors very quickly. However, the higher cost of memory is exacerbated since twice the amount of memory is required. This technique is therefore limited to applications with relatively smaller memory requirements and a very high speed priority.

A less expensive and more common solution to increasing memory reliability is to use Error Checking and Correcting (ECC) circuitry. With ECC a single bit error in a data word can be detected and corrected (also known as Single bit Error Correction (SEC)) This is especially useful in Dynamic Random Access Memory (DRAM) where soft errors may occur, that is, errors not due to the physical structure of the DRAM but due to alpha particles randomly hitting the memory chip or due to excessive noise conditions during read/write operations. When more than one bit error exists per data word detection and correction becomes substantially more complex. Double Error Detection (DED) may be provided in order to provide notice of the errors while no attempt at correction is made. Double error correction could be provided although the additional requirements for doing so are substantial.

A method of scattering errors in a memory array so as to diminish the likelihood of double errors which may be prohibitively too expensive for correction is described by Bond, et al., in U.S. Pat. No. 4,488,298. Scattering is accomplished in an array of memories by preventing two or more defective bits from aligning by selectively rearranging columns of the different memories based on an error map created for the array of memories. The error map is created off-line with each memory being tested with known data. The time to create the error map increases proportionately as the amount of memory increases. Very large memory arrays could take hours to map and scatter.

Fault mapping to determine the type of error that exists may be accomplished by storing known data in the memories (off-line) and sequentially reading the data back out and comparing it with the known written data. The errors are counted and based on the number and location of errors, the type of error is determined, i.e., single bit, bit line or word line. This method is disclosed by Ryan in U.S. Pat. No. 4,456,995. Based on the generated fault map, the bits may be scattered as described by Bond, et al. Typically, when a computer is first turned on, memory is tested one row at a time (off-line) and as each row passes it is given to the operating system to be used by the computer. As the amount of memory integrated into computers continues to expand this method becomes less desirable since testing time may become prohibitively long and the probability of an uncorrectable error occurrence continues to increase over time.

An improvement is realized by mapping errors on-line as described by Ryan in U.S. Pat. No. 4,479,214 ('214) which is hereby incorporated by reference. The system described in '214 operates much faster than the above described systems and methods. However, the speed increase comes at a cost of additional hardware. For example, 73 counters are required for a memory system having a 72 bit word, that is, one counter for each column of bits and an additional counter to keep track of the number of memory accesses so that a ratio of errors to accesses may be determined. Furthermore, the system described in '214 creates a fault map for one partition of the memory system at a time. When faults are found that would be uncorrectable by ECC the memory subsystem is then repartitioned (scattered). This reactive approach improves on test speed but requires a substantial amount of hardware and cannot identify memory that may need replacement in the future, i.e., in a preventative manner.

Thus what is needed is a fault mapping apparatus able to identify memory on-line that is likely to fail while using a minimum amount of hardware.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved on-line fault mapping apparatus for memory.

Another object of the present invention is to provide an on-line fault mapping apparatus for memory that provides a proactive indication of a memory that may need to be replaced.

Yet another object of the present invention is to provide an on-line fault mapping apparatus for memory that requires a reduced amount of hardware.

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
14	BRS	L14	7	13 and ((detect$5 determi$5) same edge)	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:28	

Still another object of the present invention is to provide an on-line fault mapping apparatus for memory that provides the mapping function by making independent maps of portions of the memory.

These and other objects of this invention are accomplished by a memory fault mapping apparatus which provides a count of errors generated by each of a plurality of memory chips. A detecting circuit checks data randomly accessed from the plurality of memory chips during on-line operation providing an indication of each error that exists in the accessed data. An error memory is coupled to the detecting circuit for storing a count of the number of errors currently detected for each memory, the count for each memory being stored in a predetermined location. A counting circuit coupled to the error memory and detecting circuit receives the count of a currently accessed memory from the error memory and if the detecting circuit indicates that an error exists, the counter increments the count. The incremented count is written back to the error memory at its predetermined location. As a result, only a single counter is required regardless of the number of bits accessed in a read operation.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of the preferred embodiment of the invention, as illustrated in the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram of a first embodiment of a fault mapping apparatus for memory according to the present invention.

FIG. 2 is a table of the error count format as stored in an error memory according to the present invention.

FIG. 3 is a block diagram of a second embodiment of a fault mapping apparatus for memory using a two pass mapping method.

FIG. 4 is a logic diagram of a first pass decoder circuit.

FIG. 4A is a logic diagram of a second pass decoder circuit.

FIG. 5 is a logic diagram of a first pass decoder circuit for a memory array having 72 bit words.

FIG. 5A is a logic diagram of a second pass decoder circuit for a memory array having 72 bit words.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 depicts a memory fault mapping apparatus 10 in block diagram form. The memory fault mapping apparatus 10 tracks the number of errors that occur in each memory chip accessed in a computer system during on-line operation. The present invention is illustrated using two memory cards 1 and 2, each having a plurality of 4 megabit memories 3. Normally much larger amounts of memory would be mapped but a smaller amount is shown for the sake of illustrative simplicity. Whenever a row of memory is accessed, the data is checked for errors and, if an error is found, the memory which generated the error is determined and a count of errors for that memory is retained. When the count for any memory reaches a predetermined magnitude remedial actions may be taken.

A decoder 5 and a decoder 7 are connected to the plurality of memories 3 with each decoder 5 and 7 receiving an address signal (row select) for selecting one row of memory of the plurality of memories 3. Further selection of the memories is made by the decoder 6 which selects one of the cards 1 or 2 from a card select address that is input to the decoder 6. The decoding step results in seven memories of the plurality of memories 3 from the cards 1 or 2 being selected for a read or write operation. During a read operation seven bits of data are made available, one bit from each of the selected memories of the plurality of memories 3 to form a seven bit ECC word (Error Checking and Correction). The seven bit ECC word is given only as an example as it is common to have larger ECC words, for example, seventy two bit ECC words are common. Three of the seven bits represent check bits and the remaining four bits represent data.

A SEC/DED syndrome generator 8 (Single Error Correct/Double Error Detect) is connected to a check bit buffer 9 by a bus 16 for receiving the three check bits. The check bit buffer 9 is connected to the plurality of memories 3 making up the three MSB (Most Significant Bits) of the seven bit ECC word. A non-zero syndrome represents that a single bit error has been detected and automatically corrected or that an uncorrected double error has been detected. A single bit error that has been corrected appears on a data bus 18 which is connected to a data buffer 11 and carries the data bits as output from the data buffer 11. The SEC/DED syndrome generator 8 outputs a three bit syndrome made up of three signals S1, S2 and S3 which form a column address signal to identify a single column from the plurality of memories 3 in which the error is detected. An error signal is also provided by the SEC/DED syndrome generator 8 which simply provides an indication that an error has been detected. For example, a "high" error signal represents an error and a "low" error signal represents the absence of an error.

An error memory 13 is a fast SRAM (Static Random Access Memory) for storing the number of errors detected in each memory of the plurality of memories 3. The error memory 13 has simultaneous read/write capability and is able to operate at twice the speed of the plurality of memories 3. There exists a corresponding memory location in the error memory 13 for each memory of the plurality of memories 3 for mapping the fault status of each such memory. Therefore the error memory 13 includes a 28 by 24 memory array (an array consisting of 28 words each having a length of 24 bits). The error memory 13 is logically split into two arrays 14 and 19 where the array 19 is 28 words by 13 bits and the array 14 is 28 words by 11 bits. The array 19 stores an error count and the array 14 stores a status word for each memory of the plurality of memories 3. Each error count and status word combine to form a fault status for a corresponding memory. The error memory 13 also includes a decoder 12 which is connected to the SEC/DED syndrome generator 8. The decoder 12 receives an address that is identical to the address of a memory of the plurality of memories 3 that has a faulty output. The address to the decoder 12 includes row select, card select and the three bit syndrome.

A counter 15 is connected to both the error memory 13 and the SEC/DED syndrome generator 8. A bus 17 having L bits connects the array 19 to the counter 15 where L is the number of bits in the error count. In the memory fault mapping system 10 the error count is composed of 13 bits so L would be equal to 13. If a larger or smaller error count were desired the value of L would reflect that number enabling the counter to receive the error count. The counter 15 receives the

	Error Definition	Errors
14		0

error count for a presently addressed memory of the plurality of memories 3 (the first 13 bits of the addressed word in error memory 13) via the bus 17. An error signal is provided to the counter 15 from the SEC/DED syndrome generator 8 for instructing the counter whether or not to increment the error count. The error count (incremented or not) is made available to the error memory 13 via the bus 17 for writing therein. The counter 15 provides a Carry Out (CO) signal, a Carry Out Minor signal (CO minor) and a Fail signal to the error memory 13. These signals update the status word of the presently addressed fault status and are described in more detail below.

METHOD OF OPERATION

The memory fault mapping apparatus 10 operates during normal computer operation or on-line. As a result, a long wait time for testing memory is not required during the initial start-up of the computer. When the computer accesses the plurality of memories 3 the row select and card select addresses are simultaneously provided to the decoders 5, 6, and 7, and to the error memory 13 via decoder 12. An ECC word from the plurality of memories 3 is then provided to the check bits buffer 9 and the data buffer 11. If a single bit error is detected in the ECC word that bit is corrected in the check bits buffer 9 and the data buffer 11. The SEC/DED syndrome generator 8 receives information regarding the status or absence of the error via bus 16. If an error was detected and corrected the three bit syndrome will reflect which column the error existed in. If no error existed, the three bit syndrome may so indicate by outputting all "zeros". By indicating the column in which an error was detected the specific memory of the plurality of memories 3 outputting the error is identified and its unique address is applied to the error memory 13. The address to the error memory 13 includes the row select and card select addresses and the three bit syndrome. As a result, each time a memory of the plurality of memories 3 outputs a detected error, an address corresponding to that memory is provided to the error memory 13.

The error memory 13 stores 28 error counts, one for each memory of the plurality of memories 3. Since an address for the faulty memory is applied to the error memory 13 the error count for that memory is output from the error memory 13 onto the bus 17 and into the counter 15. As described earlier the error signal will be "high" to indicate to the counter 15 that an error was detected. The counter 15 will thus increment the error count contained therein to reflect the current number of errors detected for the memory that produced the error. Because the error memory 13 operates at a speed at least twice that of the plurality of memories 3, the incremented error count may be written back to the error memory 13 before the current address is removed. Reading data from the plurality of memories 3 is completed in one cycle and so reading an error count, incrementing, and writing the error count back is also accomplished in a single cycle. If no error was found an invalid address is provided to the error memory 13 and the contents therein remain unchanged. After a finite time, each location in the error memory 13 contains the number of corrected single bit errors for all read operations in the memory fault mapping system 10.

The occurrence of a double error will be detected by the SEC/DED syndrome generator 8 but such an error is not indicated by the error signal and hence not counted. Instead the memory fault mapping system 10 could take other appropriate actions such as indicating that repair is necessary or make certain the addressed memory location is not used in the future. Alternative designs could embody a circuit for logically "ORing" double errors and counting one of the faulty bits. Yet another design could embody the use of double error correction circuitry and/or triple error detection.

FIG. 2 shows the format of the fault statuses stored in the error memory 13. The error count for each memory of the plurality of memories 3 are stored in the first thirteen bits of each of the 28 memory locations in the error memory 13. The error count for the memory at chip location (CHIP LOC) card 1, row 1, column 1 (1,1,1) is depicted as having a relatively low number of errors detected. Bit 13 of the error count represents the Least Significant Bit (LSB) of the binary representation of the number of errors stored therein while bit 1 is the MSB. Every time an error is detected for the memory at chip location 1,1,1 this error count is loaded into the counter 15, incremented, and the written back to the same error memory location. When an error count reaches different predetermined thresholds, symptomatic memory chip failures may be indicated. These suspected memory chip failures are indicated by the status words contained in bits 14–24 of the error memory 13.

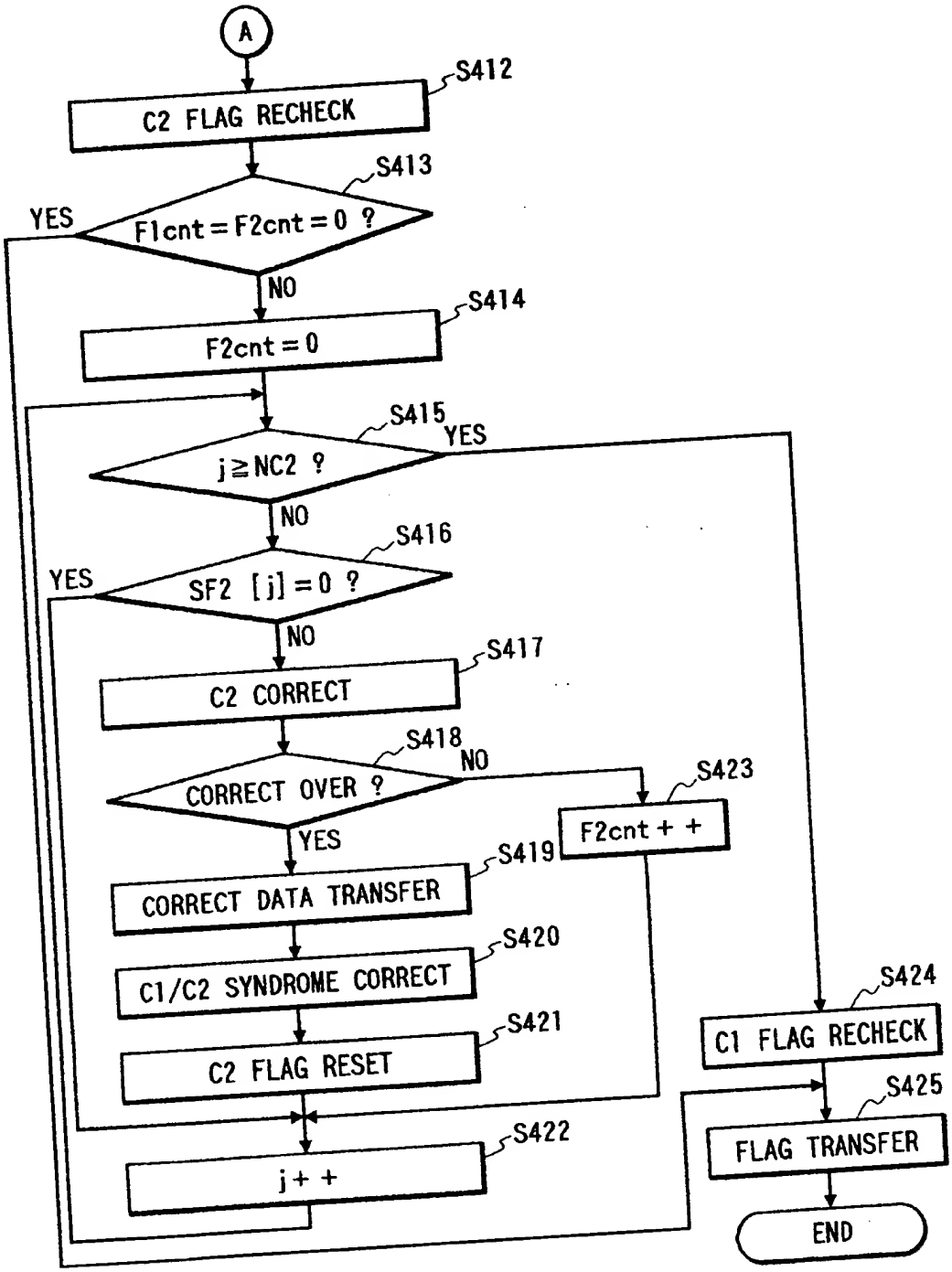
The status words contain three bits fields 14, 15, and 16 to indicate whether a chip kill, line kill or cell kill, respectively, is suspected based on the corresponding error count. The chip, line and cell kill bits are set when the corresponding error count is written back to the error memory 13. When an error count reaches a predetermined threshold, the counter 15 determines that an overflow bit has been set for a predetermined bit of that error count. The chip, line and cell kill bits are set by the CO minor, CO and fail signals supplied to the error memory 13 by the counter 15. This is illustrated by example in FIG. 2 where the error count for chip location 1,1,1 shows bit 10 as the MSB set to one and thereby causing the cell kill bit to be set. The error count for chip location 1,1,2 shows bit 3 as being the MSB set and therefore indicating a greater number of errors thereby setting the line kill bit. Likewise the error count for chip location 1,2,7 shows bit 1 as being set causing the chip kill bit to be set.

If the cell kill bit for a memory has been set, it is presumed that the errors are not due to soft errors but that that memory has a defective cell. If the higher predetermined threshold of errors has been detected for a memory such that the line kill bit has been set then a line failure will be suspected. Likewise if the still higher predetermined threshold of errors necessary to set the chip kill bit has been reached then a defective memory array module is suspected. Because the plurality of memories 3 are accessed randomly, an indication of a chip, line or cell kill will only be symptomatic. Confirmation of such a failure is accomplished, for example, by performing a sequential read for those memories having suspected defects. As a result, a memory chip that is very likely to fail in the future or that is currently defective may be found without having to test every memory of the plurality of memories 3. This provides the ability to bring a computer down for repairs at a more convenient time rather than being inconvenienced by a sudden failure.

The status words contain two bits 17 and 18 which are reserved for future use. Bit 19 is used to indicate Uncorrectable Errors (UE) as detected, for example, by

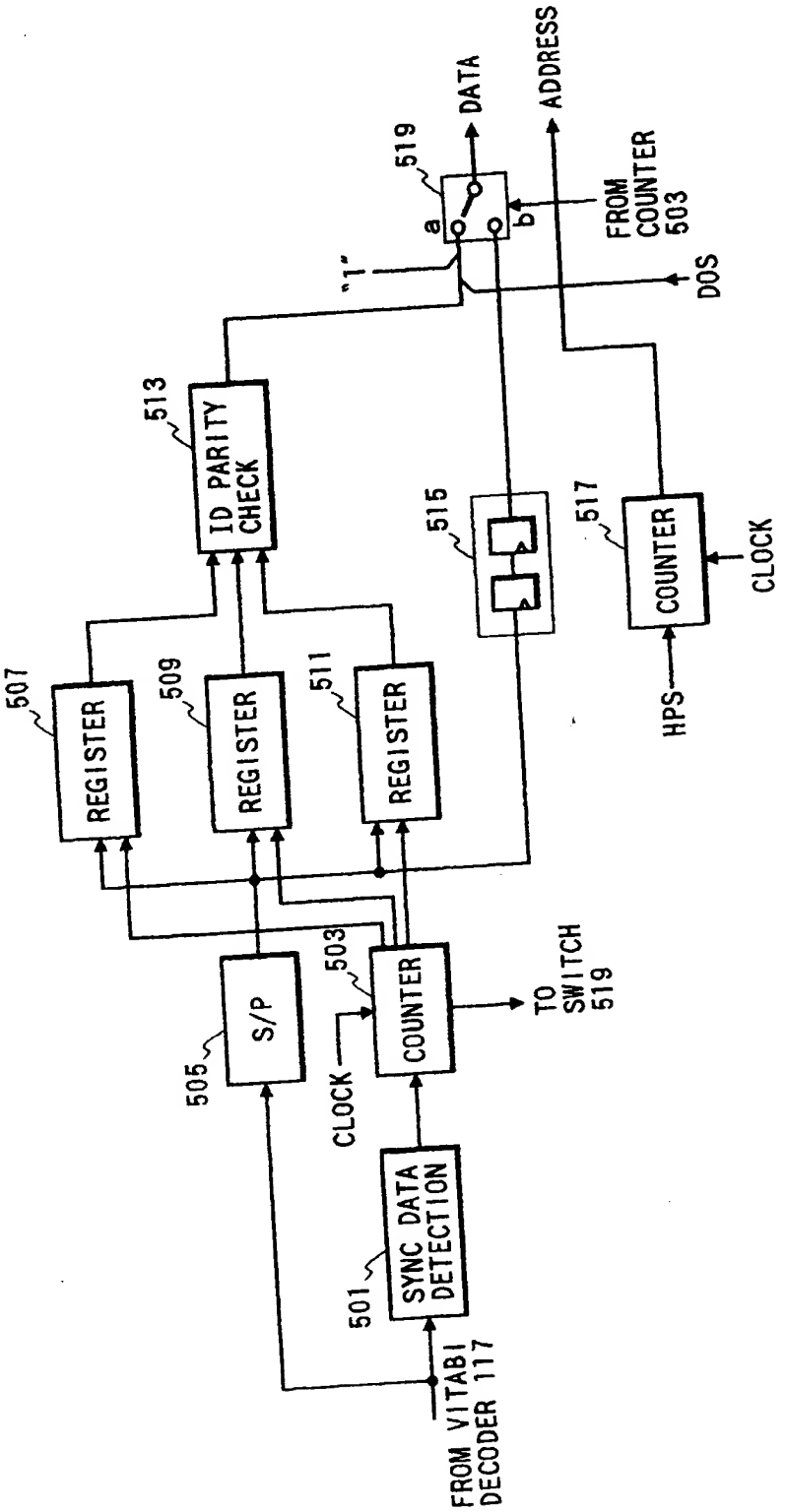
	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	20076	phase near4 error$5	USPAT	2004/02/09 15:27	
2	BRS	L2	2135	1 same (calcul$5)	USPAT	2004/02/09 15:13	
3	BRS	L4	8	3 and ((detect$5 determ$5) same edge)	USPAT	2004/02/09 15:18	
4	BRS	L7	0	4 and ((sampl$5 adj8 values) same continu$5)	USPAT	2004/02/09 15:19	
5	BRS	L8	1	4 and (calcula$5 same continu$5)	USPAT	2004/02/09 15:19	
6	BRS	L6	5	4 and (sampl$5 adj8 values)	USPAT	2004/02/09 15:23	
7	BRS	L10	2	4 and (sampl$5 same (second adj8 value$1))	USPAT	2004/02/09 15:24	
8	BRS	L9	1	4 and (sampl$5 same (first adj8 values))	USPAT	2004/02/09 15:26	
9	BRS	L11	16540	phase near4 error$5	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:27	
10	BRS	L12	1814	11 same (calcula$5)	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:27	
11	BRS	L13	54	12 same (absolute adj5 value)	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:27	

FIG. 9B


A
S412
C2 FLAG RECHECK
S413
F1cnt = F2cnt = 0 ?
YES
NO
S414
F2cnt = 0
S415
j ≧ NC2 ?
YES
NO
S416
SF2 [j] = 0 ?
YES
NO
S417
C2 CORRECT
S418
CORRECT OVER ?
NO
YES
S423
F2cnt + +
S419
CORRECT DATA TRANSFER
S420
C1/C2 SYNDROME CORRECT
S421
C2 FLAG RESET
S422
j + +
S424
C1 FLAG RECHECK
S425
FLAG TRANSFER
END

	Error Definition	Errors
1		0
2		0
3		0
4		0
5		0
6		0
7		0
8		0
9		0
10		0
11		0

FIG. 10

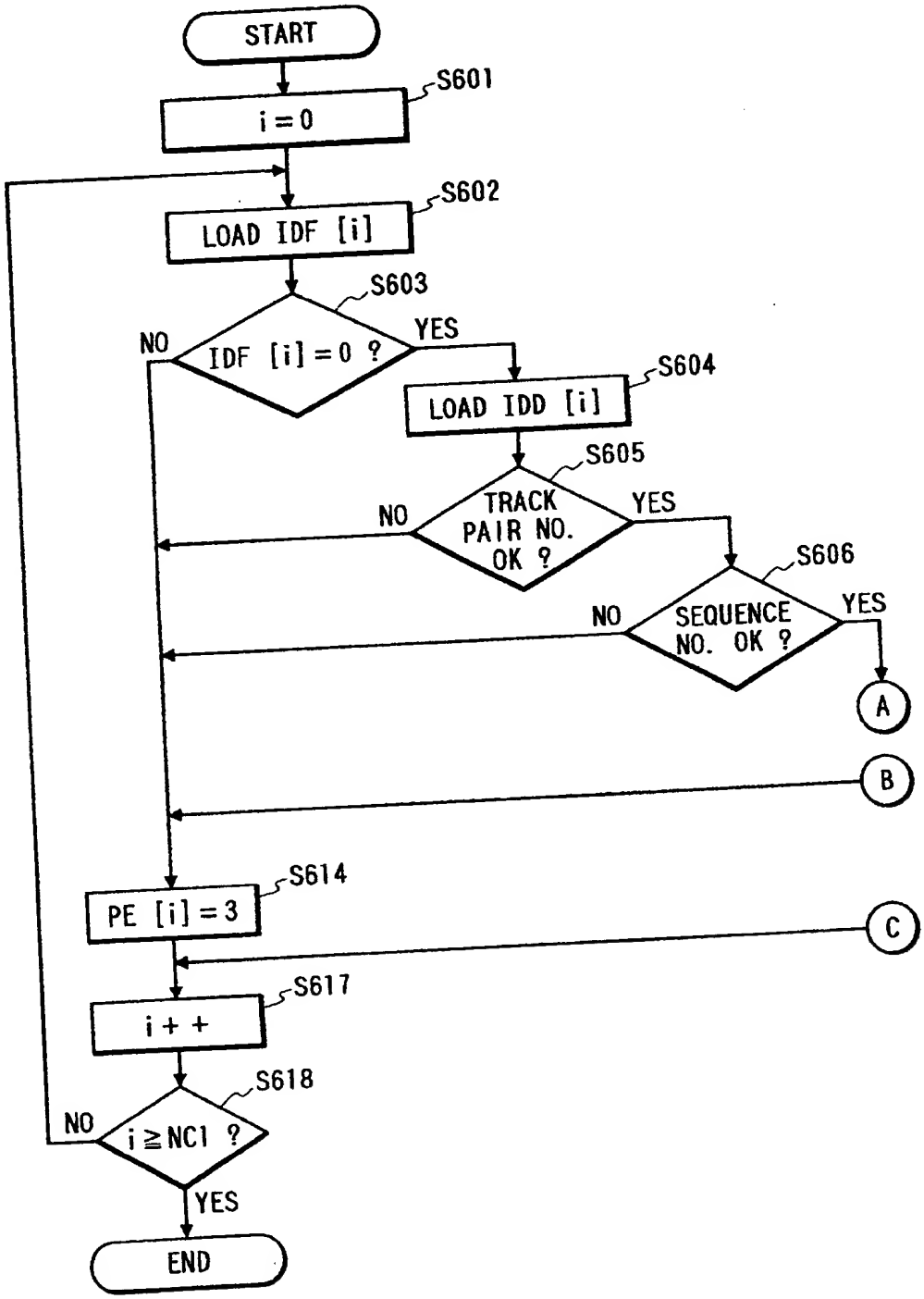

FROM VITABI DECODER 117
501
SYNC DATA DETECTION
CLOCK
505
S/P
503
COUNTER
TO SWITCH 519
507
REGISTER
509
REGISTER
511
REGISTER
513
ID PARITY CHECK
515
517
COUNTER
CLOCK
HPS
519
a
b
"1"
DOS
FROM COUNTER 503
DATA
ADDRESS

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
12	BRS	L14	7	13 and ((detect$5 determi$5) same edge)	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:28	
13	BRS	L15	24878	hamada	EPO; JPO; DERWENT	2004/02/09 15:31	
14	BRS	L16	33	15 and furuta	EPO; JPO; DERWENT	2004/02/09 15:31	
15	BRS	L17	8	16 and taguchi	EPO; JPO; DERWENT	2004/02/09 15:31	
16	BRS	L5	5	4 and (sampl$5 adj8 values)	USPAT	2004/02/09 15:36	
17	BRS	L3	77	2 same (absolute adj5 value)	USPAT	2004/02/09 15:36	
18	BRS	L18	43	3 and (sampl$5 same ((first second)third))	USPAT	2004/02/09 15:38	
19	BRS	L19	11	3 and (sampl$5 same ((first second)and third))	USPAT	2004/02/09 15:38	

FIG. 12

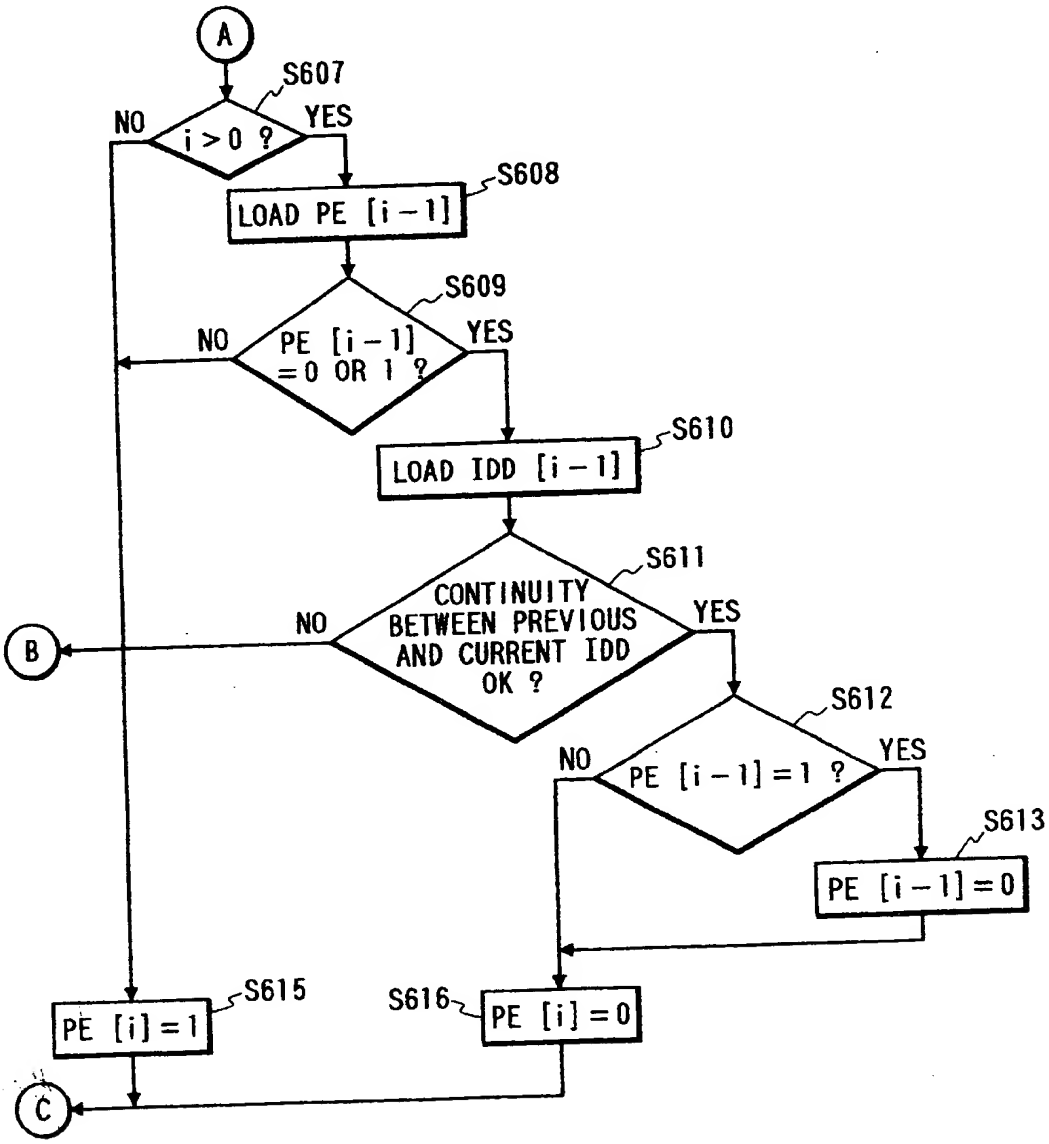
FIG. 12A	FIG. 12B

FIG. 12A



	Error Definition	Errors
12		0
13		0
14		0
15		0
16		0
17		0
18		0
19		0

FIG. 12B


A
S607
NO
i > 0 ?
YES
S608
LOAD PE [i-1]
S609
NO
PE [i-1] = 0 OR 1 ?
YES
S610
LOAD IDD [i-1]
S611
CONTINUITY BETWEEN PREVIOUS AND CURRENT IDD OK ?
NO
YES
B
S612
NO
PE [i-1] = 1 ?
YES
S613
PE [i-1] = 0
S615
PE [i] = 1
S616
PE [i] = 0
C

	Type	L #	Hits	Search Text	DBs
1	BRS	L1	143568	(((different$5 differenece) subtract$5) same sampl$4)	USPAT
2	BRS	L2	2552327	first	USPAT
3	BRS	L3	2422201	second	USPAT
4	BRS	L4	1141462	third	USPAT
5	BRS	L5	32724	1 same 2	USPAT
6	BRS	L6	19391	3 same 5	USPAT
7	BRS	L7	4029	4 same 6	USPAT
8	BRS	L8	735798	phase	USPAT
9	BRS	L9	18786	pll	USPAT
10	BRS	L10	5306	viterbi	USPAT
11	BRS	L11	2232	7 and 8	USPAT
12	BRS	L12	169	9 and 11	USPAT
13	BRS	L13	14	10 and 12	USPAT
14	BRS	L14	86322	(((different$5 differenece) subtract$5) same sampl$4)	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
15	BRS	L15	2670868	first	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

FIGS. 4*a* and 4*b* are schematic views of a conventional optical head;

FIG. 5 is a schematic view of a prism comprising a dichroic mirror and a mirror which are integrated;

FIG. 6 is a schematic view of an optical head showing the second embodiment of the present invention;

FIG. 7 is a schematic view of a conventional optical head;

FIG. 8 is a schematic view of a conventional optical head;

FIG. 9 is a block diagram of an optical disk unit showing the third embodiment of the present invention;

FIG. 10 is a schematic view for explaining the optical system of a conventional optical head;

FIGS. 11*a* and 11*b* are drawings showing the constitution of an objective lens having a hologram;

FIGS. 12*a* and 12*b* are schematic drawings showing an exchange device of an objective lens; and

FIG. 13 is an illustration for a light flux conversion device.

DETAILED EXPLANATION OF THE PREFERRED EMBODIMENTS

The constitution, operation, and effects of an optical head showing the first embodiment of the present invention will be explained hereunder with reference to the accompanying drawings.

FIGS. 1*a* and 1*b* are schematic views of an optical head showing an embodiment of the present invention. A light source **1** is, for example, a semiconductor laser diode and the light output thereof has a short wave length corresponding to a high density disk **8** such as a DVD, for example, 650 nm. A half mirror **2** leads light reflected from an information recording surface **81** of the high density disk **8** to the detection lens system **10**. A collimator lens **3** converts the divergent light outputted from the light source **1** to a parallel light flux. A mirror **4** converts a light flux traveling in the direction perpendicular to the optical axis of an objective lens **7** so as to travel in the direction of the optical axis of the objective lens **7**. A semiconductor laser module **5** comprises a light source having a different wave length from that of the light source **1** and a photo detector which are integrated. The wave length of light output by the semiconductor laser module **5** has a wave length corresponding to a normal disk **9** and longer than that of the light source **1** corresponding to the high density disk **8**, for example, 780 nm. The optical distance from the light emission point to the objective lens **7** is set so that the divergent angle of a light flux entering the objective lens **7** becomes appropriate.

A dichroic mirror **6** in the shape of a parallel flat plate is, for example, an optical element having a high transmittance and reflection factor—wave length dependence as shown in FIG. **2** and, in this case, a dichroic mirror having a high reflection factor at a wave length of 780 nm and a high transmittance at a wave length of 650 nm is used. The dichroic mirror **6** synthesizes (makes the optical axes coincide with each other) light entering from the mirror **4** and light flux entering from the laser module **5** and leads them to the objective lens **7**.

Reflected light fluxes from the information recording surfaces of the disks **8** and **9** enter the dichroic mirror **6** via the objective lens **7**. The dichroic mirror **6** reflects and leads the light flux with a long wave length from the disk **9** to the laser module **5** and passes and leads the light flux with a short wave length from the disk **8** to the mirror **4**.

The objective lens **7** is designed to focus a parallel light flux with a wave length of 650 nm of the light source **1** with satisfactory aberration via a disk board with a thickness of 0.6 mm. A transparent protective film **82** is formed on the surface of the disk board and light transmits the protective film **82** and is reflected on the information recording surface **81**. In normal use, when a light flux with a wave length of 780 nm of the laser module **5** passes a disk board with a thickness of 1.2 mm using the objective lens **7**, spherical aberration increases. Therefore, the light flux cannot be focused on an information recording surface **91** of the normal disk **9** with satisfactory aberration.

However, depending on the divergent angle of a light flux entering the objective lens **7**, it is possible to cancel the spherical aberration caused by differences in the disk thickness and wave length and obtain a satisfactory spot. The aforementioned laser module **5** is arranged in a position where the divergent angle of a light flux entering the objective lens **7** is given so as to form a satisfactory spot on the information recording surface **91** of the normal disk **9** with a corresponding wave length of 780 nm at a thickness of 1.2 mm using the objective lens **7**.

The high density disk **8** is 0.6 mm in thickness and the corresponding wave length is a 650-nm band. The normal disk **9** is 1.2 mm in thickness and the corresponding wave length is longer that of the high density disk **8** such as a 780-nm band. A detector optics **10** is provided so as to detect light reflected from the high density disk **8**.

When the astigmatism method is used for focus control, the detector optics **10** comprises a cylinder lens and others. A photo detector **11** using a photodiode detects a reproduced signal as well as a control signal for controlling the focusing position.

The aforementioned embodiment uses the light source **1**, the half mirror **2**, the detection lens system **10**, and the photo detector **11**. However, these may have the same constitution as that of the semiconductor module **5**. In this case, the optical axis of the high density optical system (corresponding to high density disk **8**) is parallel with the optical axis of the CD optical system (corresponding to high density disk **9**). The operation of an optical head having the aforementioned constitution when data is recorded or reproduced on or from the high density disk **8** will be explained hereunder.

The light source **1** is turned on and the laser module **5** is turned off. Almost 50% of a light flux outputted from the light source **1** is reflected from the half mirror **2**, changes its beam direction, enters the collimator lens **3**, and is converted to a parallel light flux. The parallel light flux reflects from the mirror **4** and goes toward the dichroic mirror **6**. The dichroic mirror **6** has a high transmittance for a light flux with a wave length of 650 nm, so that the incident light flux transmits as it is, enters the objective lens **7**, and focuses on the information recording surface **81** of the high density disk **8** with satisfactory aberration.

The light flux reflected from the information recording surface **81** of the high density disk **8** transmits the objective lens **7** and the dichroic mirror **6** and then reflects from the mirror **4** and enters the collimator lens **3**. The light flux is converted to a converged light flux by the collimator lens **3** and enters the half mirror **2** and almost 50% thereof transmits it and is led to the detector optics **10** and then reaches the photo detector **11**, and a reproduced signal and a control signal are detected.

The operation when the normal disk **9** is recorded or reproduced will be explained hereunder.

The light source **1** is turned off and the laser module **5** is turned on. A light flux outputted from the laser module **5**